# High-Frequency Capacitor with Working Substance “Insulator–Undoped Silicon–Insulator”

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The study of the parameters of capacitors with various working substances is of interest for the design and creation of electronic elements, in particular for the development of high-frequency phase-shifting circuits.

The purpose of the work is to calculate the high-frequency capacitance of a capacitor with the working substance “insulator–undoped silicon–insulator” at different applied to the capacitor direct current (DC) voltages, measuring signal frequencies and temperatures.

A model of such the capacitor is proposed, in which 30 μm thick layer of undoped (intrinsic) crystalline silicon (*i*-Si) is separated from each of the capacitor electrodes by 1 μm thick insulator layer (silicon dioxide).

The dependences of the capacitor capacitance on the DC electrical voltage $U$ on metal electrodes at zero frequency and at the measuring signal frequency of 1 MHz at absolute temperatures $T = 300$ and 400 K are calculated. It is shown that the real part of the capacitor capacitance increases monotonically, while the imaginary part is negative and non-monotonically depends on $U$ at the temperature $T = 300$ K. An increase in the real part of the capacitor capacitance up to the geometric capacitance of oxide layers with increasing temperature is due to a decrease in the electrical resistance of *i*-Si layer. As a result, with an increase in temperature up to 400 K, the real and imaginary parts of the capacitance take constant values independent of $U$. The capacitance of *i*-Si layer with an increase in both temperature $T$ and voltage $U$ is shunted by the electrical conductivity of this layer. The phase shift is determined for a sinusoidal electrical signal with a frequency of 0.3, 1, 10, 30, 100, and 300 MHz applied to the capacitor at temperatures 300 and 400 K.

**Keywords:** undoped (intrinsic) crystalline silicon, silicon dioxide, capacitance, three-layer flat capacitor.

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# Высокочастотный конденсатор с рабочим веществом «изолятор – нелегированный кремний – изолятор»

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Исследование параметров электрических конденсаторов с различными рабочими веществами представляет интерес для проектирования и создания элементов электроники, в частности для разработки высокочастотных фазосдвигающих цепей.

Цель работы – рассчитать высокочастотную электрическую емкость конденсатора с рабочим веществом «изолятор – нелегированный кремний – изолятор» при различных подаваемых на конденсатор постоянных напряжениях, частотах измерительного сигнала и температурах.

Предложена модель такого конденсатора, в которой слой нелегированного (собственного) кристаллического кремния (*i*-Si) толщиной 30 мкм отделен от каждого из электродов конденсатора слоем изолятора (диоксида кремния) толщиной 1 мкм.

Рассчитаны зависимости емкости конденсатора от постоянного электрического напряжения $U$ на металлических электродах на нулевой частоте и на частоте измерительного сигнала 1 МГц при абсолютных температурах $T = 300$ и 400 К. Показано, что действительная часть емкости конденсатора монотонно возрастает, а мнимая часть отрицательна и немонотонно зависит от $U$ при температуре $T = 300$ К. Увеличение действительной части емкости конденсатора до геометрической емкости оксидных слоев при увеличении температуры обусловлено уменьшением электрического сопротивления слоя *i*-Si. Вследствие этого с увеличением температуры до 400 К действительная и мнимая части емкости принимают постоянные значения, независящие от $U$. Емкость слоя *i*-Si при увеличении как температуры $T$, так и напряжения $U$ шунтируется электрической проводимостью этого слоя. Определен сдвиг фаз для синусоидального электрического сигнала с частотой 0,3; 1; 10; 30; 100 и 300 МГц, подаваемого на конденсатор при температурах 300 и 400 К.

**Ключевые слова:** нелегированный (собственный) кристаллический кремний, диоксид кремния, электрическая емкость, трехслойный плоский электрический конденсатор.

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## Introduction

Nonlinear screening of an external stationary electric field in materials occurs when the density of the charge induced by the field in them is not proportional to the total electrostatic potential of the field and charges. An analytical and numerical solution of the problem of nonlinear screening of an impurity ion by a spherically symmetric cloud of mobile charges of opposite sign in covalent crystalline semiconductors is given in [1]. It was also noted there that the concept of nonlinear screening can be justified only when the root-mean-square fluctuations of the potential energy of mobile uncompensated charges are less than the thermal energy for nondegenerate semiconductors and less than the Fermi energy for degenerate semiconductors. With nonlinear screening of an external electrostatic field, alternating layers with nonequilibrium (due to illumination) electrons and holes can appear in a "semi-infinite" semiconductor [2]. It is also possible that a three-layer structure "negatively charged layer–electrically neutral layer–positively charged layer" appears in a gas plasma located in a strong electric field between metal electrodes (cathode and anode) [3].

In work [4] low-frequency electrical losses in *n*-type crystalline silicon placed in a capacitor with deep impurity energy levels were studied. The low-frequency admittance and the phase shift angle between the sinusoidal current and voltage in the capacitor with the working substance "insulator–partially disordered silicon–insulator" were calculated in [5]. The frequency dependence of the admittance and the nonlinear capacitance on the voltage of the "semiconductor–insulator–metal–insulator–semiconductor" structure, which simulates semiconductor materials with metallic nanosized inclusions, was also theoretically studied [6]. However, the temperature dependences of the admittance and capacitance of such a structure were not calculated. The influence of the process of formation of electrically neutral pairs of defects from electrically charged defects on the chaotic electrostatic potential on the surface of a semiconductor was studied [7], and the conditions for strong localization of a two-dimensional electron gas on the surface in the presence of this potential were determined [8].

In work [9], the differential capacitance of a semiconductor film with an ohmic contact on the back side was calculated. The distribution of the electrostatic potential induced by an external stationary electric field over the thickness of a semiconductor film deposited on an insulator is considered in [10], and on a metal in [11]. In Refs. [12, 13], the working substance "insulator–intrinsic semiconductor–insulator" of a low-frequency capacitor was considered, however, the calculation of the frequency and temperature dependences of its capacitance was not carried out. Thus, the calculation of the high-frequency electrophysical characteristics of a capacitor with an undoped semiconductor separated by insulating layers from its metal plates is still an urgent task in electronics. This is important for building a theory of phase-shifting electrical circuits with a nonlinear capacitor.

Here we note that in [14], the possibility of implementing an electrical analogue of Rayleigh–Bénard cells in a flat capacitor "insulator–nondegenerate *n*-type semiconductor–insulator" by creating a stationary electric potential difference between its metal plates was theoretically studied. These cells represent ring electron currents in the semiconductor cross section, which seems important for the study of synergistic electronic states and processes in device structures.

The purpose of the work is to calculate the high-frequency capacitance of a capacitor with the working substance "insulator–undoped crystalline silicon–insulator" at different applied to the capacitor direct current (DC) voltages, measuring signal frequencies and temperatures. Silicon dioxide is considered as an insulator.

## Equivalent circuit of three-layer capacitor

Let a layer of undoped (intrinsic) crystalline semiconductor (*i*-Si) with thickness $L_s$ and side surface area $A$ be located in the middle between metal plates of a flat electric capacitor and separated from them by insulator layers ($SiO_2$); see Figure 1*a*. The capacitor is connected to a DC voltage source $U$. There is no electric charge at the $SiO_2$/*i*-Si interfaces at $U = 0$. The $x$ axis of the Cartesian coordinate system is perpendicular to the surface of *i*-Si layer occupying the space $0 < x < L_s$; the $y$ and $z$ axes are parallel to the layer surface. Let us assume that in one part of *i*-Si layer the potential of the external stationary electric field on the surface is positive $\varphi(x = 0) = +\varphi_s/2$, and in the other part it is negative $\varphi(x = L_s) = -\varphi_s/2$. Then the electric potential difference applied to the semiconductor layer is

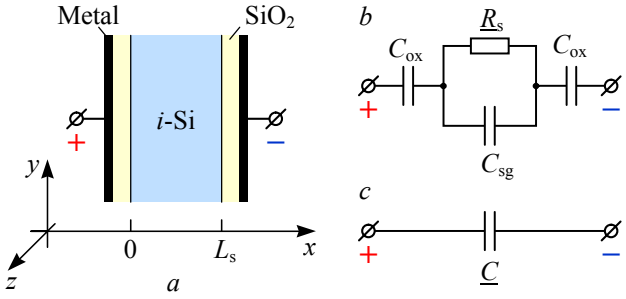


**Figure 1** – Cross section of a capacitor with a layer of intrinsic crystalline semiconductor (*i*-Si) of thickness $L_s$ and area $A$ in $yz$ plane; semiconductor is separated from metal plates (electrodes) by insulator layers ($SiO_2$) of thickness of $L_{ox}$. Across the semiconductor layer (along $x$ axis), an electric potential difference is applied between two electrodes (anode and cathode) parallel to $yz$ plane (*a*). Equivalent circuit of the device structure (*b*). Simplified equivalent circuit of the device structure (*c*)

$U_s = \varphi(x=0) - \varphi(x=L_s) = \varphi_s$. The electrodes are parallel to the $yz$ plane, so that the electric potential $\varphi$ depends only on $x$ and is independent of $y$ and $z$. Screening of the external electrostatic field is due to the redistribution of electrons in the *c*-band and holes in the *v*-band inside *i*-Si layer.

The capacitor with the working substance "silicon dioxide–intrinsic silicon–silicon dioxide" contains a parallel $\underline{R}_s C_{sg}$-circuit of *i*-Si layer, connected in series with the capacitances of the $C_{ox}$ insulating layers (see Figure 1*b*). Here, the complex electrical resistance of the semiconductor layer $\underline{R}_s = \underline{R}_s(U_s,\omega) = R_{s1}(U_s,\omega) - \mathrm{i}\,R_{s2}(U_s,\omega)$, $\mathrm{i} = (-1)^{1/2}$ is the imaginary unit, $C_{sg} = C_s + C_g$ is the electrical capacitance of the semiconductor, $C_{ox} = A\varepsilon_{ox}/L_{ox}$ and $C_g = A\varepsilon_s/L_s$ are the geometric capacitances of a single $SiO_2$ layer and *i*-Si layer with static permittivities $\varepsilon_{ox} = \varepsilon_{rox}\varepsilon_0$ and $\varepsilon_s = \varepsilon_{rs}\varepsilon_0$; $\varepsilon_{rox}$ and $\varepsilon_{rs}$ are the relative permittivities of $SiO_2$ and *i*-Si, respectively, $\varepsilon_0 = 8.85$ pF/m is the electrical constant, $C_s = C_s(U_s)$ is the differential capacitance of the semiconductor, $U_s$ is the voltage across the semiconductor. In the equivalent circuit (Figure 1*c*), the capacitance $\underline{C} = \underline{C}(U,\omega)$ of the capacitor depends on the DC voltage $U$ and the angular frequency $\omega$ of the measuring signal.

The real $C_1$ and imaginary $C_2$ parts of the complex capacitance $\underline{C} = \underline{C}(U,\omega) = C_1(U,\omega) + \mathrm{i}\,C_2(U,\omega)$ of the equivalent circuit (see Figure 1*c*) are [15–17]:

$$C_1 = \mathrm{Re}\,\underline{C} = \frac{C_{ox}}{2\Xi}\left[1 + \omega R_{s2}(C_{ox}/2 + 2C_{sg}) + \omega^2(R_{s1}^2 + R_{s2}^2)C_{sg}(C_{ox}/2 + C_{sg})\right], \quad (1)$$

$$C_2 = \mathrm{Im}\,\underline{C} = \frac{-\omega R_{s1}(C_{ox}/2)^2}{\Xi} < 0,$$

where

$$\Xi = [1 + \omega R_{s2}(C_{ox}/2 + C_{sg})]^2 + \omega^2 R_{s1}^2(C_{ox}/2 + C_{sg})^2,$$

$U\,(=U_{dc})$ is the stationary electric voltage on metal plates of the capacitor, $\omega$ is the angular frequency of the alternating current (AC) component of the measuring signal with the amplitude $|U_{ac}| \ll U_{dc}$; $R_{s1} > 0$ and $R_{s2} > 0$; see Eq. (13) below.

The real $Y_1$ and imaginary $Y_2$ parts of the complex admittance $\underline{Y} = \underline{Y}(U,\omega) = Y_1 + \mathrm{i}\,Y_2$ of the capacitor equivalent circuit (Figure 1*c*) are:

$$Y_1 = \mathrm{Re}\,\underline{Y} = -\omega C_2, \quad Y_2 = \mathrm{Im}\,\underline{Y} = \omega C_1. \quad (2)$$

From Eq. (2) we find the phase shift $\theta = \theta(U,\omega)$ between the alternating current and the voltage on the capacitor with the working substance "insulator–intrincis silicon–insulator" as

$$\theta = \arctan(-Y_2/Y_1) = \arctan(C_1/C_2). \quad (3)$$

Formulas (1)–(3) are transformed into formulas from Refs. [5, 18] if $\underline{R}_s$ does not depend on the measuring signal frequency $\omega$.

Since the capacitances of the insulator layers ($C_{ox}$) and *i*-Si layer ($C_{sg}$) are connected in series (see Figure 1*b*), the charge on each of the layers is equal to $Q$. Then the complex voltage drops on the insulators $\underline{U}_{ox} = Q/C_{ox}$ and on the intrinsic silicon $\underline{U}_s = Q/(C_{sg} + 1/\mathrm{i}\omega\underline{R}_s)$ are related to the complex capacitor voltage $\underline{U}$ as $\underline{U} = 2\underline{U}_{ox} + \underline{U}_s$. To find the value of $\underline{U}$, we substitute the charge $Q$ on the capacitor, expressed in terms of $\underline{U}_s$ and $(C_{sg} + 1/\mathrm{i}\omega\underline{R}_s)$, into $\underline{U}_{ox}$ and take the modulus of the complex voltage $U = |\underline{U}| = |2\underline{U}_{ox} + \underline{U}_s|$. As a result, we obtain the ratio of the voltage across the entire capacitor $U$ to the voltage across the semiconductor $U_s = |\underline{U}_s|$ as

$$\frac{U}{U_s} = \frac{2}{C_{ox}}\left[\left(C_{sg} + \frac{C_{ox}}{2} + \frac{R_{s2}}{\xi}\right)^2 + \left(\frac{R_{s1}}{\xi}\right)^2\right]^{1/2}, \quad (4)$$

where $\xi = \omega(R_{s1}^2 + R_{s2}^2)$.

Let us consider a layer of undoped (intrinsic) crystalline silicon with volume $V_s = AL_s$, which contains equal concentrations of *c*-band electrons (symbol and index $n$) and *v*-band holes (symbol and index $p$) with bulk concentrations (see, e.g., [19, 20]):

$$n = \frac{1}{V_s}\int_0^\infty g_n f_n \,\mathrm{d}E_n = n_c F_{1/2}\left(\frac{E_F^{(c)}}{k_B T}\right) = n_c F_{1/2}(\eta_c),$$
$$p = \frac{1}{V_s}\int_0^\infty g_p f_p \,\mathrm{d}E_p = p_v F_{1/2}\left(\frac{E_F^{(v)}}{k_B T}\right) = p_v F_{1/2}(\eta_v), \quad (5)$$

where the energy densities of states of electrons in the *c*-band and holes in the *v*-band are

$g_n = V_s(2m_{nd})^{3/2}E_n^{1/2}/2\pi^2\hbar^3$,
$g_p = V_s(2m_{pd})^{3/2}E_p^{1/2}/2\pi^2\hbar^3$;

$m_{nd}$, $E_n$ and $m_{pd}$, $E_p$ are the effective masses of the density of states and the kinetic energy of $c$-band electron and $v$-band hole; $\hbar = h/2\pi$ is the Planck constant; the Fermi–Dirac distribution functions for electrons and holes are

$f_n = \{1 + \exp[(E_n - E_F^{(c)})/k_BT]\}^{-1}$,
$f_p = \{1 + \exp[(E_F^{(v)} - E_p)/k_BT]\}^{-1}$;

$E_F^{(c)} < 0$ and $E_F^{(v)} < 0$ are the positions of the Fermi level counted from the bottom of the $c$-band and the top of the $v$-band; $-(E_F^{(c)} + E_F^{(v)}) = E_g > 0$ is the width of the energy gap ($i$-Si band gap); $k_B$ is the Boltzmann constant; $T$ is the absolute temperature;

$n_c = 2(2\pi m_{nd}k_BT)^{3/2}/(2\pi\hbar)^3$;
$p_v = 2(2\pi m_{pd}k_BT)^{3/2}/(2\pi\hbar)^3$;

Fermi–Dirac integral (of index 1/2):

$$F_{1/2}(\eta_{c(v)}) = \frac{2}{\sqrt{\pi}}\int_0^\infty \sqrt{\chi}[1 + \exp(\chi - \eta_{c(v)})]^{-1}\,d\chi.$$

Distribution of space charge density $\rho(x)$ of $v$-band holes with concentration $p(x)$ and $c$-band electrons with concentration $n(x)$ along $x$ axis when an external DC voltage $U$ ($= U_{dc}$) is applied to metal electrodes (plates) of the capacitor taking into account Eq. (5) is given by the expression:

$$\rho(x) = e[p(x) - n(x)] = e\left[p_v F_{1/2}\left(\frac{E_F^{(v)}(x)}{k_BT}\right) - n_c F_{1/2}\left(\frac{E_F^{(c)}(x)}{k_BT}\right)\right], \quad (6)$$

where $e$ is the elementary charge, $E_F^{(v)}(x) = E_F^{(v)} - e\varphi(x)$ and $E_F^{(c)}(x) = -[E_g + E_F^{(v)}(x)]$ are the positions of the Fermi level relative to the top of the $v$-band and the bottom of the $c$-band in an electric field with potential $\varphi(x)$.

Note that for a nondegenerate gas of $c$-band electrons and $v$-band holes the following inequalities hold: $E_F^{(c)}(x) < 0$, $|E_F^{(c)}(x)| > 3k_BT$ and $E_F^{(v)}(x) < 0$, $|E_F^{(v)}(x)| > 3k_BT$. Under these conditions, the Fermi–Dirac energy distribution functions of electrons and holes transform into the Maxwell–Boltzmann distribution functions [20, 21]. In this case, the space charge density distribution (6) over the thickness of $i$-Si layer takes the form (see, e.g., [22, 23]):

$$\rho(x) = -2en_i\sinh(e\varphi(x)/k_BT),$$

where $n_i = p_i$ is the concentration of $c$-band electrons (equal to the concentration of $v$-band holes) in $i$-Si layer at $U = 0$.

The electrical neutrality condition for $i$-type silicon in the absence of an external field ($U = 0$), when $E_F^{(c)}$ and $E_F^{(v)}$ do not depend on $x$ coordinate, has the form:

$$n_i = p_i = [n_c p_v \exp(-E_g/k_BT)]^{1/2}. \quad (7)$$

The electrostatic potential $\varphi(x)$ at the point with coordinate $x$ inside $i$-Si with the volume density of the induced charge $\rho(x)$ satisfies the Poisson equation [19, 20]:

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{\rho(\varphi(x))}{\varepsilon_{rs}\varepsilon_0}, \quad (8)$$

where the charge density $\rho(x) = \rho(\varphi(x))$ is determined by Eq. (6), the value of the potential on the semiconductor surface is determined by the boundary conditions: $\varphi(x = 0) = +\varphi_s/2$ and $\varphi(x = L_s) = -\varphi_s/2$.

From the solution of the Poisson equation (8), we obtain the charge $Q_s$ induced by the external electric field per unit area $A$ of the flat surface of $i$-Si layer:

$$\frac{Q_s}{A} = \int_{L_s/2}^{L_s} \rho(\varphi(x))\,dx. \quad (9)$$

The differential capacitance per unit area $A$ of $i$-Si surface, taking into account Eqs. (6)–(9), is

$$\frac{C_s}{A} = -\frac{dQ_s}{A\,d\varphi_s} = A\frac{\varepsilon_s\rho(-\varphi_s/2)}{Q_s(-\varphi_s/2)}, \quad (10)$$

where the volume charge density $\rho(-\varphi_s/2)$ is determined by Eq. (6), and the charge $Q_s(-\varphi_s/2)$ is determined by Eq. (9).

Stationary (DC) electrical conductivity of $i$-Si layer, due to the migration of electrons and holes across the layer thickness, is

$$\sigma_{dc} = \sigma_{dcn} + \sigma_{dcp},$$
$$\sigma_{dcn} = \frac{e\mu_n}{L_s}\int_0^{L_s} n(x)\,dx, \quad \sigma_{dcp} = \frac{e\mu_p}{L_s}\int_0^{L_s} p(x)\,dx, \quad (11)$$

where $\sigma_{dcn}$ and $\sigma_{dcp}$ are the electron and hole DC electrical conductivities, $n(x)$ and $p(x)$ are the concentrations of $c$-band electrons and $v$-band holes given by Eqs. (5), $\mu_n$ and $\mu_p$ are the drift mobilities of electrons and holes.

Here we note that the drift mobilities of electrons and holes in undoped silicon are limited by phonon scattering and, under isothermal conditions, do not depend on the coordinate.

AC electrical conductivity of $i$-type crystalline silicon according to the Drude–Lorentz model, taking into account Eq. (11), is (see, e.g., [19, 20]):

*Table*

**Parameters of intrinsic (undoped) crystalline silicon**

| $T$, K | $E_g$, eV | $m_{nd}/m_0$ | $m_{pd}/m_0$ | $m_{n\sigma}/m_0$ | $m_{p\sigma}/m_0$ | $\mu_n$, $cm^2 \cdot V^{-1} \cdot s^{-1}$ | $\mu_p$, $cm^2 \cdot V^{-1} \cdot s^{-1}$ | $n_i$, $cm^{-3}$ | $\varepsilon_{rs}$ | Reference |
|---|---|---|---|---|---|---|---|---|---|---|
| 300 | 1.12 | 1.062 | – | 0.259 | – | 1750 | 450 | – | 11.6 | [24] |
| | 1.1242 | 1.062 | 1.161 | 0.259 | 0.708 | 1450 | 505 | $1.02 \cdot 10^{10}$ | 11.9 | [25] |
| | 1.12 | 1.08 | 0.81 | 0.26 | – | 1400 | 450 | $1 \cdot 10^{10}$ | 11.7 | [26] |
| | 1.12 | 1.09 | 1.001 | – | – | – | – | $9.65 \cdot 10^{9}$ | – | [27] |
| | 1.12 | 1.09 | – | – | – | 1430 | 480 | $1.07 \cdot 10^{10}$ | – | [28] |
| 400 | 1.095 | – | – | – | – | – | 251 | – | – | [24] |
| | 1.098 | – | 1.239 | – | 0.746 | 722 | 251 | – | – | [25] |
| | 1.097 | – | – | – | – | 759 | 263 | $1.65 \cdot 10^{12}$ | – | [26] |
| | – | 1.109 | 1.068 | – | – | – | – | $1.87 \cdot 10^{12}$ | – | [27] |
| | 1.0968 | 1.11 | – | – | – | 697 | 234 | $6.00 \cdot 10^{12}$ | – | [28] |

*Note:* $E_g$ is the band gap, $m_{nd}$ and $m_{pd}$ are the effective masses of the density of states of $c$-band electrons and $v$-band holes, $m_{n\sigma}$ and $m_{p\sigma}$ are the effective masses of the electrical conductivity of electrons and holes, $\mu_n$ and $\mu_p$ are the drift mobilities of electrons and holes, $n_i$ is the intrinsic electron concentration equal to the intrinsic hole concentration $p_i$, $\varepsilon_{rs}$ is the relative permittivity of intrinsic silicon at absolute temperatures $T = 300$ and 400 K; here $m_0$ is the electron mass in vacuum.

$$\begin{gathered}\sigma_{ac} = \sigma_1 + i\sigma_2 = \sigma_{1n} + \sigma_{1p} + i(\sigma_{2n} + \sigma_{2p}),\\ \sigma_{1n} = \sigma_{dcn}/[1 + (\omega\tau_n)^2],\ \sigma_{2n} = \sigma_{dcn}\omega\tau_n/[1 + (\omega\tau_n)^2],\\ \sigma_{1p} = \sigma_{dcp}/[1 + (\omega\tau_p)^2],\ \sigma_{2p} = \sigma_{dcp}\omega\tau_p/[1 + (\omega\tau_p)^2],\end{gathered} \quad (12)$$

where $\tau_n = \mu_n m_{n\sigma}/e$ and $\tau_p = \mu_p m_{p\sigma}/e$ are the quasi-momentum relaxation times of average $c$-band electron and average $v$-band hole when they scatter on phonons of $i$-type silicon crystal lattice, $m_{n\sigma}$ and $m_{p\sigma}$ are the effective masses of the electrical conductivity of $c$-band electrons and $v$-band holes, $\omega$ is the angular frequency of the measuring signal.

From Eq. (12) we obtain the complex electrical resistance of undoped silicon in the form:

$$\begin{gathered}\underline{R}_s = \frac{L_s}{A}\frac{1}{\sigma_{ac}} = R_{s1} - iR_{s2},\\ R_{s1} = \frac{L_s}{A}\frac{\sigma_1}{\sigma_1^2 + \sigma_2^2},\quad R_{s2} = \frac{L_s}{A}\frac{\sigma_2}{\sigma_1^2 + \sigma_2^2},\end{gathered} \quad (13)$$

where $\sigma_1 = \sigma_{1n} + \sigma_{1p}$ and $\sigma_2 = \sigma_{2n} + \sigma_{2p}$.

## Calculation results and discussion

The calculations of capacitances $C_1$ and $C_2$ were performed for the parameters [24–28] of undoped silicon ($i$-Si) indicated in Table for its thickness $L_s = 30$ μm and measuring signal frequencies $\omega/2\pi = 0.3$, 1, 30, 100, and 300 MHz. Relative permittivity of silicon dioxide ($SiO_2$) $\varepsilon_{rox} = 3.9$ and its thickness $L_{ox} = 1$ μm. In the calculations it was assumed that the capacitor is under isothermal conditions.

The electrical voltage of the external field on the whole structure should not exceed breakdown field voltage of silicon dioxide ($SiO_2$) $U_{bd}$, where $U_{bd}$ is the experimentally measured threshold breakdown voltage of $SiO_2$ of thickness $L_{ox}$. Thus, the voltage $U$ must satisfy the condition $U < U_{bd}$, where $U_{bd} \approx 0.4$–1 kV for silicon dioxide of thickness $L_{ox} = 1$ μm at a stationary external breakdown electric field strength $E_{bd} = 4$–10 MV/cm [29–31].

Figure 2 shows the dependence of the voltage $U_s$ across $i$-Si layer of thickness $L_s = 30$ μm according to Eq. (4) on the voltage $U$ (created by metal electrodes of the capacitor on the surface of each of two $SiO_2$ interlayers of thickness $L_{ox} = 1$ μm) for measuring

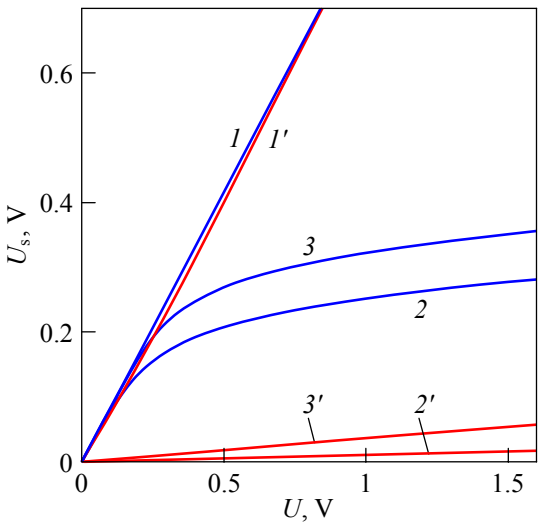


**Figure 2** – Dependence of electrical voltage $U_s$ across $i$-Si of thickness $L_s = 30$ μm on stationary voltage $U$ on the capacitor electrodes for $L_{ox} = 1$ μm according Eq. (4), at frequency $\omega/2\pi$, MHz: 0 (curves *1*, *1′*), 0.3 (*2*, *2′*) and 1 (*3*, *3′*) at $T$, K: 300 (blue lines *1–3*) and 400 (red lines *1′–3′*)

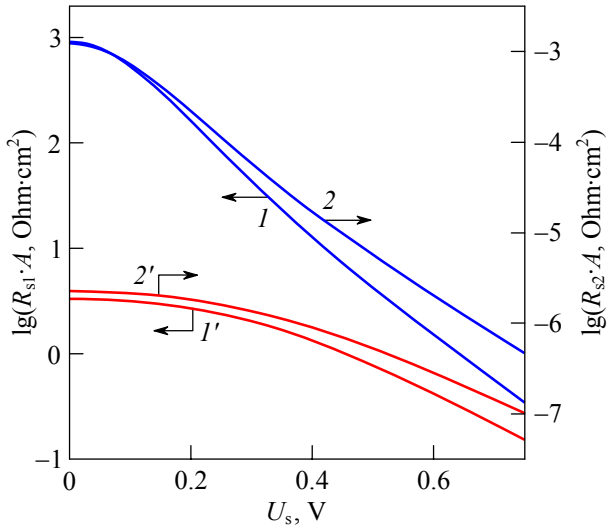


**Figure 3** – Dependence of decimal logarithm of real $\lg(R_{s1}\cdot A$, Ohm·cm$^2$) (curves *1*, *1′*) and imaginary $\lg(R_{s2}\cdot A$, Ohm·cm$^2$) (curves *2*, *2′*) parts of complex resistance of *i*-Si layer at frequency $\omega/2\pi = 1$ MHz on electrical voltage $U_s$ across the layer; calculation by Eqs. (13) for $L_s = 30$ μm at $T$, K: 300 (blue lines *1*, *2*) and 400 (red lines *1′*, *2′*)

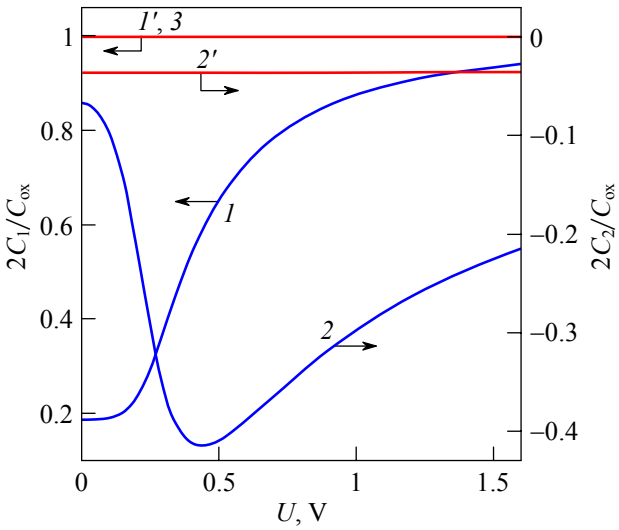


**Figure 4** – Dependence of real $2C_1/C_{ox}$ (curves *1*, *1′*, *3*) and imaginary $2C_2/C_{ox}$ (*2*, *2′*) parts of complex capacitance on voltage $U$ at the capacitor electrodes, calculated by Eqs. (1) for $L_s = 30$ μm and $L_{ox} = 1$ μm at $T$, K: 300 (blue lines *1*, *2*) and 400 (red lines *1′*, *2′*) and $\omega/2\pi$, MHz: 0 (curve *3*) and 1 (curves *1*, *1′*, *2*, *2′*)

signal frequencies $\omega/2\pi$ = 0, 0.3, and 1 MHz at temperatures $T = 300$ and 400 K. It is seen that at constant voltage across the capacitor contacts ($U$ = const), the voltage drop $U_s$ across *i*-Si layer decreases with temperature.

Figure 3 shows the dependences of the real $R_{s1}$ and imaginary $R_{s2}$ parts of the electrical resistance of *i*-Si layer according to Eqs. (13) on the DC voltage $U_s$ across this layer for measuring signal frequency $\omega/2\pi = 1$ MHz at temperatures $T = 300$ and 400 K. It is seen that the electrical resistance of *i*-Si layer decreases with temperature and voltage.

Figure 4 shows the results of calculating the ratio of the real $C_1(U,\omega)$ and imaginary $C_2(U,\omega)$ parts of the complex capacitance to the capacitance of the insulating layers $C_{ox}/2$ according to Eq. (1). The calculation was performed for different values of voltage $U$ (created by metal electrodes of the capacitor on the surface of $SiO_2$ insulating interlayers, each of thickness $L_{ox} = 1$ μm) for semiconductor of thickness $L_s = 30$ μm at absolute temperatures $T = 300$ and 400 K and measuring signal frequencies $\omega/2\pi$ = = 0 and 1 MHz. As the temperature $T$ increases, the concentrations of electrons and holes increase (see Table), which leads to a decrease in the electrical resistance of *i*-Si layer and, as a result, to an increase in capacitances $C_1$ and $C_2$. As the voltage $U$ increases, the capacitance $C_1$ increases monotonically, while the capacitance $C_2$ changes non-monotonically. This is due to the displacement of the majority of

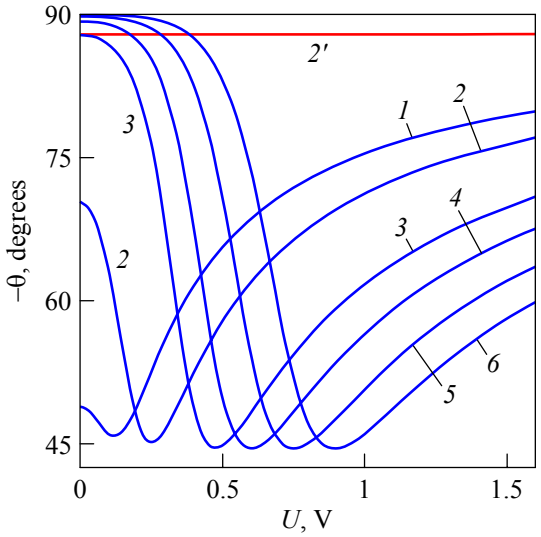


**Figure 5** – Dependence of measuring signal phase shift angle θ at frequency $\omega/2\pi$ on stationary voltage $U$ at the capacitor electrodes, calculated by Eq. (3) for $L_s = 30$ μm and $L_{ox} = 1$ μm at $T = 300$ K (blue lines); $\omega/2\pi$ (MHz) = = 0.3 (curve *1*), 1 (*2*), 10 (*3*), 30 (*4*), 100 (*5*), 300 (6) and at temperature $T = 400$ K (red line *2′* for $\omega/2\pi = 1$ MHz)

electrons to $SiO_2$ insulating layer adjacent to the anode, and the majority of holes to $SiO_2$ insulating layer adjacent to the cathode.

Figure 5 shows the results of calculating the dependences of the phase shift angle θ between the alternating current and measuring signal voltage according to Eq. (3) on the constant voltage $U$ (created by metal electrodes of the capacitor on the surface of $SiO_2$ interlayers) at the absolute temperature

$T = 300$ K for frequencies $\omega/2\pi$ = 0.3, 1, 10, 30, 100, and 300 MHz and at $T = 400$ K for $\omega/2\pi$ = = 1 MHz. It is seen that with an increase in temperature $T$, other things being equal, the phase shift angle modulus $|\theta|$ increases. With an increase in the voltage $U$ on metal electrodes, the calculation gives a non-monotonic dependence of the phase shift angle $\theta$ on $U$.

Note that, according to Eq. (3), the maximum value of $-\pi/4$ (= $-45°$) is reached by the quantity $-\pi/2 \le \theta \le 0$ at such an angular frequency $\omega$ when the equality $Y_2 = Y_1$ (or $C_1 = -C_2$) is satisfied.

## Conclusion

A theoretical model of high-frequency capacitor with the working substance "silicon dioxide–intrinsic silicon–silicon dioxide" is developed. A 30 μm thick semiconductor layer of *i*-type crystalline silicon is separated on both sides from metal plates of the capacitor by 1 μm thick insulating layers of silicon dioxide.

The numerical calculation shows that the real part of the capacitance increases monotonically with voltage at the capacitor electrodes while the imaginary part is negative and non-monotonically depends on the voltage at measuring signal frequency of $\omega/2\pi = 1$ MHz at the temperature $T = 300$ K. It is shown that at the temperature $T = 400$ K the real and imaginary parts of the capacitance of the capacitor take constant values, independent of voltage, which is due to a decrease in the electrical resistance of *i*-Si layer. The capacitance of *i*-Si layer with an increase in both the temperature $T$ and the DC voltage $U$ for frequencies $\omega/2\pi \le 1$ MHz is shunted by the electrical conductivity of this layer.

The dependence of the phase shift angle on the voltage of a sinusoidal electrical signal applied to the capacitor for frequencies of 0.3, 1, 10, 30, 100, and 300 MHz at temperatures 300 and 400 K is calculated. It is shown that as the signal frequency increases, the minimum of the phase shift angle modulus shift towards higher voltages, and at a frequency of 1 MHz, with an increase in temperature to 400 K, it reaches a constant value. Note that if a narrow-gap *i*-InSb is used as an undoped (intrinsic) semiconductor, then such a capacitor will operate at cryogenic temperatures.

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