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IF-DECISION DIAGRAM BASED GENERATION OF PARALLEL ADDERS

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Works [1-4] proposed a new class of decision diagrams, i.e. IFDs that are based on a theory of incompletely specified Boolean functions.

A one-bit full-adder (Figure 1, left) adds three one-bit numbers a , b and c_{in} , and produces two one-bit numbers s and c_{out} . Figure 1, right shows a two-root if-decision diagram (IFD) that models the adder. The incoming edges of roots are labeled with s and c_1 . The diagram consists of three nonterminal nodes and seven terminal nodes. The nonterminal node is not labeled and has three outgoing edges. The terminal node has no outgoing edges and is labeled by a variable a , b and c_0 , or a variable negation (\neg).

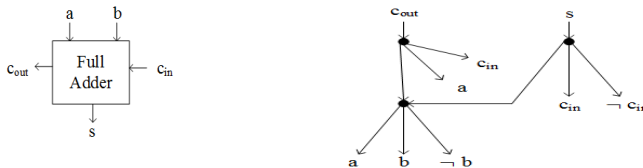


Fig.1. One-bit full-adder and its IFD-based modelling

The one-bit full-adder allows the construction of an N -bit ripple carry adder (RCA). Figure 2 depicts a 8-root IFD that realizes the 7-bit adder. The diagram consists of two-type nonterminal nodes: *xor* and *if-then*

else. While the advantage of the adder IFD is a regular structure and a low cost of 21 nonterminal nodes, its drawback is a large-time delay that is determined by the IFD critical path of 8 nonterminal nodes.

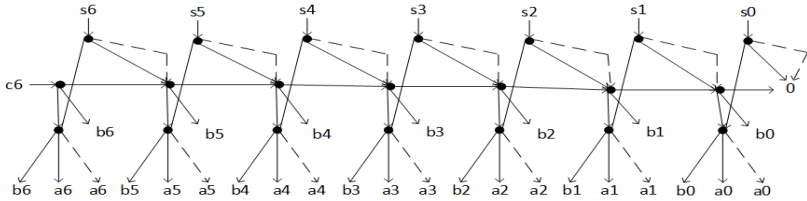


Fig. 2. IFD of 7-bit ripple carry adder

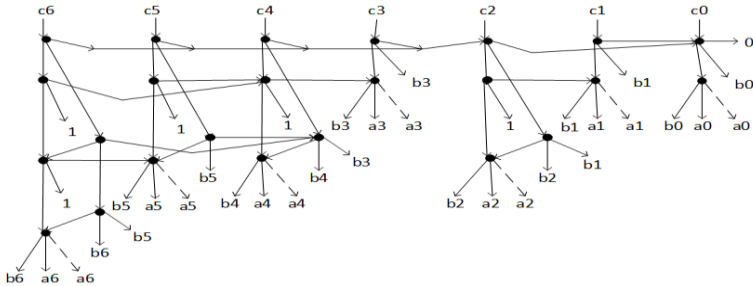


Fig. 3. IFD of carry part of 7-bit parallel adder

The goal of the paper is to create a procedure of systematical generation of IFDs of faster parallel many-bit adders [5] from the RCA IFD. Work [6] develops a method of cutting long paths in a many-root IFD to obtain a new IFD with shorter critical paths. The depth of the new IFD is lower, but its sizes slightly grows. Figure 3 depicts an IFD of the carry part of a 7-bit parallel adder. The diagram size is 24 nodes against 14 nodes in RCA, and the diagram depth is 4 nodes against 8 nodes in RCA.

Figure 4 depicts a five-block-structure of the IFD of the 31-bit carry part of the parallel adder. Blocks 0, 1, 2, 3 and 4 have the bit-size of 1, 2, 4, 8 and 16 respectively. Figure 4 also reports in parentheses the

block-depth of 2, 3, 4, 5 and 6, and the node count of 2, 4, 6, 8 and 10 for the left bit of each block.

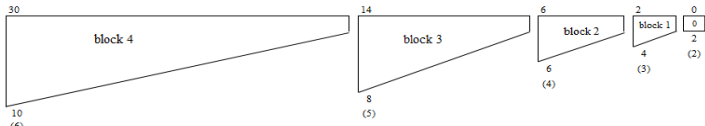


Fig. 4. Five-block carry part of 31-bit parallel adder

Based on the experience of systematically transforming IFDs of various-bit ripple carry adders to IFDs of parallel adders, we have found out that it is possible to develop an efficient algorithm of automatically generating a parallel n -bit-adder IFD at any finite n . The algorithm is based on a recursive procedure, which is capable of generating the IFD of block i from the IFD of block $i-1$. Figure 5 shows how we construct the IFD of block 4 from the IFD of block 3 in a 31-bit adder.

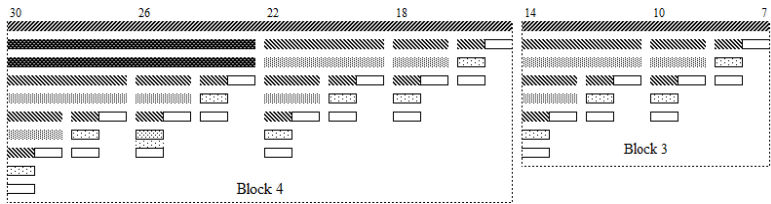


Fig.5. Construction of block 4 IFD over block 3 IFD in 31-bit adder

A horizontal line represents a set of nodes, which refer over the third outgoing edge to the node located right to the line. For instance, the top line of block 4 represents nodes from bit 15 to bit 30, and all these nodes refer over the third outgoing edge to a node of bit 14. Observing Figure 5, we can see that block 4 consists of two copies of block 3, one located in bits 15 – 22, and other located in bits 23 – 30. Two additional node lines (in dark) are inserted between lines 1 and 2 in the second copy of block 3. In both block copies, the variable indices are re-enumerated as well as the referred node indices.

In Figure 5, filled in dark horizontal rectangles represent sets of nodes that have horizontal and vertical references to other nodes. The lightly filled cells have only vertical references, and the cells without fill have no any references.

The described algorithm of recursively constructing blocks that is applied many times to IFDs is capable of generating a parallel adder of any bit-width. We can estimate the IFD-size of the n -bit parallel adder as

$$S^{pr}(n) = n + (n + 1) \times \log_2(n + 1) \quad (1)$$

We can estimate the IFD-depth of the n -bit parallel adder as

$$D^{pr}(n) = 1 + \log_2(n + 1) \quad (2)$$

Figure 6 shows how the average and maximal number of IFD nodes in the parallel adder carry part grows depending on the adder bit-width. At the bit-width of 1023, the depth of parallel adder almost 100 times lower the depth of RCA, and its size is higher only 5 times.

The parallel adder generation algorithm is capable of creating IFD structures that can be mapped to reversible digital circuits for further quantum implementation [7].

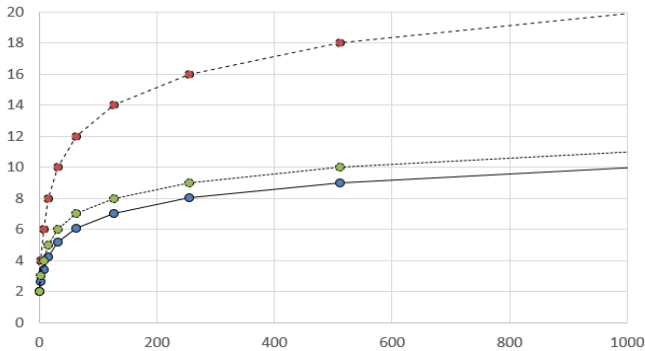


Fig. 6. Average (solid) and maximal (dash) size per bit and depth (square dot) of carry part IFD vs. adder width

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